

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KRAMADHATI V. RAVI, KENT ROSSMAN,
TURGUT SAHIN, and PRAVIN NARWANKAR

Appeal 2007-0299
Application 09/362,504
Technology Center 1700

Decided: March 29, 2007

Before EDWARD C. KIMLIN, BRADLEY R. GARRIS, and PETER F. KRATZ, *Administrative Patent Judges*.

KRATZ, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal from the Examiner's final rejection of claims 16-36. We have jurisdiction pursuant to 35 U.S.C. §§ 6 and 134.

Appellants' invention is directed to an integrated circuit comprising two film layers formed on a substrate, a substrate processing system, a computer readable storage medium including computer readable instructions (code), and a high-density chemical vapor deposition system. Claims 16, 17, 20, 23, and 32 are illustrative and reproduced below:

16. An integrated circuit formed on a semiconductor substrate by the method of:

- a) flowing a process gas into a substrate processing chamber;
- b) forming a plasma from said process gas by coupling sputtering energy into said substrate processing chamber;
- c) thereafter, maintaining said plasma to deposit a first layer of a film over said substrate by sputtering without biasing said plasma toward said substrate; and
- d) thereafter, maintaining said plasma by maintaining coupling of said sputtering energy into said substrate processing chamber and biasing said plasma toward said substrate to deposit a second layer of said film over said first layer.

17. A substrate processing system comprising:

- a housing for forming a vacuum chamber;
- a vacuum pump for evacuating said vacuum chamber;
- a pedestal, located within said housing, configured to hold a substrate;
- a gas distribution system fluidly coupled to said vacuum chamber;
- a plasma generation system for forming a plasma from process gas within said vacuum chamber and for selectively biasing said plasma toward said substrate;
- a controller for controlling said vacuum pump, said gas distribution system and said plasma generation system;

a memory coupled to said controller and storing a program for directing the operation of said system, said program including a set of instructions for depositing a film by first, controlling said gas distribution system to introduce said process gas into said chamber;

second, controlling said plasma generation system to form a plasma from said process gas by coupling sputtering energy into said vacuum chamber and deposit a first layer of said film over said substrate by sputtering without biasing said plasma towards said substrate; and

third, controlling said plasma generation system to maintain said plasma by maintaining coupling of said sputtering energy into said vacuum chamber and bias said plasma toward said substrate to deposit a second layer of said film over said first layer.

20. A high-density plasma chemical vapor deposition system comprising:

a housing for forming a vacuum chamber; a pedestal, located within said housing, for holding a substrate; means for introducing reactants into said vacuum chamber; means for generating a plasma from said reactants by applying a sputtering power to said reactants to deposit a first layer of a film on said substrate during a first time period, said first layer for the reduction of mechanical stress in a subsequently deposited layer of a silicon oxide film; and

means for biasing said plasma toward said substrate during a second time period after said first time period to enhance a sputtering of said plasma while maintaining application of said sputtering power to said reactants and deposit said subsequent layer.

23. An integrated circuit formed on a semiconductor substrate, said integrated circuit comprising:

(a) a plurality of active devices formed in said semiconductor substrate;

(b) at least one metal layer formed above said semiconductor substrate; and

(c) at least one insulating layer formed between said metal layer and said semiconductor substrate, said insulating layer having a plurality of patterned holes filled with electrically conductive material to electrically connect selected portions of said metal layer to selected portions of said semiconductor substrate, wherein said insulating layer comprises a first silicon oxide layer and a second silicon oxide layer, said first and said second silicon oxide layers deposited using a high-density plasma chemical vapor deposition process, said first silicon oxide layer deposited for the reduction of mechanical stress in said second silicon oxide layer.

32. A computer readable storage medium having program code embodied therein, said program code for controlling a substrate processing system, wherein said substrate processing system includes a processing chamber, a gas delivery system, a plasma generation system and a controller configured to control the gas delivery system and the plasma generation system said program code controlling the semiconductor processing system to process a wafer in the chamber in accordance with the following:

- (i) a first set of computer instructions for controlling the gas delivery system to introduce a process gas into the processing chamber;
- (ii) a second set of computer instructions for controlling the plasma generation system to form a plasma from the process gas by coupling sputtering energy into said processing chamber to deposit a first layer of a film over a substrate by sputtering without biasing said plasma towards said substrate; and
- (iii) a third set of computer instructions for controlling said plasma generation system to maintain said plasma by maintaining coupling of said sputtering energy into said processing chamber and to bias said plasma toward said substrate to deposit a second layer of said film over said first layer.

The Examiner relies on the following references as evidence of the prior art in rejecting the appealed claims:

Boys	US 4,500,408	Feb. 19, 1985
Matsuura	US 5,319,247	Jun. 7, 1994
Li	US 5,772,771	Jun. 30, 1998

Jin Onuki et al. (Onuki), "High-reliability interconnection formation by a two-step switching bias sputtering process," 266 *Thin Solid Films* 182-88 (1995)

Claim 16 stands rejected under 35 U.S.C. § 102 as being anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over Onuki. Claims 17-19, 31, and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Boys in view of Onuki. Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Li in view of Onuki. Claims 21 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Li in view of Onuki and Boys. Claims 23, 24, and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Onuki in view of Matsura. Claims 25-30, 33, 34, and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Boys and Onuki in view of Li.

We affirm the Examiner's separate rejections of claim 16, claim 20, and claims 21 and 22. We reverse the remaining rejections. Our reasoning follows:

Rejection of Claim 16

At the outset, we note that the integrated circuit product of appealed claim 16 is described, at least in part, by a process of preparing same. In assessing the patentability of such a product-by-process claim, the product made is the focus of our inquiry. In this regard, the patentability of a product is a separate consideration from that of the process by which it is made. *See In re Thorpe*, 777 F.2d 695, 697, 227 USPQ 964, 966 (Fed. Cir. 1985); *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972).

The Examiner has found that Onuki teaches or suggests an integrated circuit that includes multiple film layers deposited on a substrate (Answer 3-5). The deposit is made via the use of a plasma that is struck with

alternating application of sputtering power and applied bias (Onuki, Fig. 4). Appellants maintain that Onuki does not teach forming a layer (corresponding to the claimed second layer) while maintaining coupling of sputtering energy and the application of bias of the plasma toward the substrate in addition to forming a layer (corresponding to the claimed first layer) using sputtering energy without the plasma being biased (Br. 8).

We agree with Appellants that Onuki does not explicitly describe Appellants' claimed sequence of power application. In particular, the sputtering power is seemingly turned off during the bias application when a sequential power application operation is conducted as shown in the drawing figures of Onuki (*see*, for example, Fig. 1b). However, the product, not the process of making, is at issue. In this regard, we note that appealed claim 16 does not require any particular amount of bias and/or sputtering energy to be applied in forming the layers called for therein. Nor does appealed claim 16 limit the other processes and apparatus parameters associated with the formation of a plasma, deposit of the layers, or otherwise limit the characteristics and composition of the two layers being deposited. For example, Onuki shows that bias voltage influences the argon (Ar) content of a deposited aluminum alloy film. However, zero bias voltage is shown as resulting in substantially the same Ar content in the film as a negative bias voltage between 50 and 100 Volts (Onuki, Fig. 3). Thus, this disclosure of Onuki seemingly supports the Examiner's assertion that the layers of claim 16, which are formed under zero bias and other than zero bias conditions, are not required to be materially different from each other even though deposited under the argued different conditions (Answer 20).

Given this record, we determine that the Examiner has established the making of an integrated circuit with a film deposit by Onuki, which appears to be sufficiently like the film deposit broadly called for in claim 16 as to suggest the claimed integrated circuit film. A fair and reasonable assessment of the evidence (Onuki) supplied by the Examiner warrants a shifting of the burden of production of contrary evidence on this point to Appellants. Indeed, this evidence production requirement of Appellants is appropriate given the product-by-process nature of appealed claim 16, the Examiner's rejection over prior art that teaches a film deposited via the application of a plasma and sputtering, and given that the arguments made in favor of the patentability of the product made are primarily limited to asserted process distinctions. This is so in order for Appellants to establish that the argued process distinction respecting the conditions under which bias and sputtering energy are employed together in depositing a second layer, as an addition to sputtering without bias in forming a first layer, actually requires a product distinction over Onuki's deposited layers. After all, Appellants are in a better position than the Patent and Trademark Office to carry out such comparative testing.

We note that Appellants' assertion of an intrinsic stress characteristic for the first layer is unavailing because claim 16 does not specify a particular, much less a patentably distinguishing, stress reduction property for the first layer. Additionally, claim 16 does not explicitly specify any particular composition or associated characteristics required for the deposited layers. Also, the record does not reflect the production of substantiating persuasive evidence corresponding with arguments made by Appellants in the Briefs that would establish a patentably distinct

characteristic for Appellants' product based on the method of preparing same recited in claim 16.

It follows that we sustain the Examiner's anticipation and alternative obviousness rejection of claim 16 over Onuki, on this record.

Rejection of Claim 20

Claim 20 is drawn to a high-density plasma chemical vapor deposition (HDP-CVD) system.

Li discloses a system for HDP-CVD that substantially corresponds to the claimed system including:

- (a) a housing forming a vacuum chamber (2);
- (b) a pedestal for holding a substrate located within the reaction chamber (14);
- (c) a reactant inlet (70, 34, 38);
- (d) a plasma generation system applying sputtering power to reactants introduced into the chamber including an RF generator (10), a circuit (12), and an inductive coil (8); and
- (e) a biasing system including an RF generator (22) and circuit (24) connected to the pedestal (14), and an RF generator (26), and circuit (28) connected to the chamber housing top (25). *See* Fig. 1 of Li and the corresponding text.

Appellants' only dispute with the application of the HDP-CVD apparatus of Li as corresponding to the apparatus of claim 20 is based on the contention that "Li . . . [does] not disclose a controller or a memory storing a program for directing the operation of the system to deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma" (Br. 12). We disagree with the assumption underlying this argument – an

assumption that claim 20 includes a limitation requiring a controller or memory storing an operating program with instructions as recited.

Claim 20 includes several means plus function limitations for which Appellants have presented information in their Brief as to the corresponding subject matter disclosed in their specification which they believe is conveyed thereby under the sixth paragraph of 35 U.S.C. § 112. None of these recited means limitations reasonably requires a computer controller with a programmed memory based on the record before us.

In particular, we note that the “means for generating a plasma . . .” of claim 20 is described by Appellants as requiring a coiled antenna (26), and an RF generator (32) connected thereto via a switch (34), or an equivalent thereof. *See Br. 4.* We agree with that assessment of Appellants as no programmed memory or controller storing a program is invoked by this language. Indeed, Appellants’ processor (31) or memory (33), as illustrated in drawing figure 1 of the application, is not mentioned by Appellants as being the specification structure corresponding to this means plus function element. Nor have Appellants otherwise argued that the coiled antenna (8), RF generator (10), and matching connecting circuit (12) of Li do not reasonably correspond to the structure Appellants present as being called for by the “means for generating a plasma . . .” of claim 20.

Similarly, the “means for biasing . . .” of claim 20 does not require a programmed processor or memory. Rather, the corresponding structure from the specification this latter means is directed to is indicated by Appellants as including a plasma chamber cover electrode (24), bias RF generator (36) and connecting switch (38), and (possibly or) a chuck (44), bias RF generator (50) and connecting switch (52). See the paragraph

bridging pages 4 and 5 of the Specification and the corresponding elements in the drawing Fig. 1. We agree that such listed structures and equivalents thereof are required by this latter means clause, not a programmed memory or programmed controller. Appellants do not otherwise contest that this means clause requires structure other than the bias structure disclosed or suggested by Li. See cover electrode (25), RF generator (26), and connecting circuit (28), as well as chuck electrode (40), RF generator (22), and connecting electrode (24) of Li.

Moreover, we are confident that our determination of the scope of 20, as not including a programmed memory controller and/or programmed memory, represents a fair and broadest reasonable construction of the pending application claims before us. That is, our claim construction is believed to be consistent with current patent jurisprudence and takes appropriate account of the application specification and drawings as would be understood by one of ordinary skill in the art in assessing the scope of claim 20. *See Gechter v. Davidson*, 116 F.3d 1454, 1457, 43 USPQ2d 1030, 1032 (Fed. Cir. 1997); *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997); *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). Here, one of ordinary skill in the art would readily recognize that Appellants did not intend to require a programmed controller or memory as part of the structure corresponding to either of these means plus function limitations or any other element of the claim 20 apparatus. After all, such control could be accomplished through manually operable switches. For example, an operator could measure the first time period during which the sputtering power is applied, as well as the second time period for applying biasing power rather than employing a programmed

computer. Accordingly, we determine that claim 20 is drawn to apparatus without any requirement for stored programming and an automatic controller being installed as part of the apparatus and such as to require that the controller and installed program code mandates a particular operating sequence. Because we determine that the structure required by claim 20 has not been shown to patentably distinguish over the structure taught or suggested by Li, we need not reach the additional teachings of Onuki, as additionally applied by the Examiner.

It follows that we will sustain the Examiner's obviousness rejection of claim 20, on this record.

Rejection of Claims 21 and 22

In a separate obviousness rejection of claims 21 and 22, which depend from claim 20, the Examiner additionally relies on the teachings of Boys. Appellants do not argue the Examiner's application of Boys to the additional features of these dependent claims in the rejection of these claims. Rather, Appellants rely on their arguments against independent claim 20 (Br. 12). We find those arguments unpersuasive for reasons discussed above. Accordingly, we also affirm the Examiner's rejection of claims 21 and 22, on this record.

Rejection of Claims 17-19, 31, and 32

Our disposition of the Examiner's rejection of these claims stands on a different footing than our treatment of the Examiner's rejections of claims 20-22. This is because a particularly programmed and functional computer readable memory (independent claim 32) and an apparatus including a controller connected to such a programmed memory (independent claim 17) are part of the required subject matter being claimed at here. Consequently,

the Examiner's reliance on Onuki to suggest a modification of the system of Boys is clearly at issue.

Like Appellants, however, we can find no clear direction in Onuki which would have suggested a modification to the apparatus or computer readable memory of Boys that would result in a particularly programmed product or apparatus, as being claimed at as at least part of the subject matter of these rejected claims.

Boys is directed to an apparatus and method for controlling sputter coating. Boys employs a magnetron-type sputter coating device. The sputter coating device includes a vacuum chamber (12), a target cathode (15), anode (16), a substrate (14), and a plasma generating gas supply and power source. An inert gas, such as argon, is supplied to a volume inside the sputter coating device of Boys and a plasma is struck using DC plasma source current (37). A coil power source (25) is also employed to vary a magnetic field applied to an assembly (17), including the target cathode (15). Magnetic (fringing flux) field lines (25)¹ and electrical field lines (38) are formed at right angles to each other. See Fig. 1 and the corresponding textual description of the apparatus of Boys.

Boys discloses controlling the sputter apparatus and coating deposition using, *inter alia*, plasma parameters, such as desired operating voltage and desired operating current for a given plasma power as well as a desired operating pressure to control the coating operation. In particular, Boys is concerned with controlling the magnetron sputter coating apparatus to control deposition, including the deposition profile of sputtering material

¹ Boys employs reference numeral (25) to denote both a DC power source and magnetic flux lines.

on a substrate as the target erodes. Plasma parameters are used to control magnetic field intensity and, in turn, electrical impedance of the plasma (col. 4, ll. 1-10).

Several proportional integral differential (PID) controller loops are part of the control apparatus of Boys. A first PID loop (Loop # 2, Fig. 3) is designed to allow for operation at a predetermined plasma voltage, as the target erodes, via constant control of the electromagnetic coil current so as to vary the fringing field intensity, and resulting in control of the plasma impedance (col. 4, ll. 29-33). According to Boys, “[t]he plasma current is controlled independently of the plasma voltage in response to the output of a second PID loop . . . ; the second PID loop effectively controls plasma power” (col. 4, ll. 21-26). Loop #3 of drawing Figure 3 corresponds to this second described PID loop. A third PID loop (Loop # 1, Fig. 3) is employed in controlling the plasma pressure via control of gas flow rate. A CPU (57, Fig. 1) with a programmable memory is employed, in effecting an automatic control of the deposition via the above-noted PID loops. *See* col. 8, l. 43 through col. 9, l. 46 of Boys.

Thus, Boys is concerned with an automatic control of a magnetron sputter system to achieve a desired deposition, including a desired deposition rate and deposition profile on a substrate, while taking the non-uniform wear of a planar emitting surface of a target into account (col. 9, l. 47 – col. 11, l. 59). *See* Fig. 1 of Boys and the corresponding text of the applied patent.

With that general description of the complex control system of the magnetron sputtering system of Boys in mind, the examiner correctly recognizes that Boys does not teach a computer readable storage medium or controller memory that is programmed with instructions for controlling

sputtering energy coupling with and without biasing for depositing second and first layers, respectively, on a substrate, as required by the rejected claims (independent claims 17 and 32). *See Answer 7-10.* The Examiner maintains, however, that (Answer 10):

[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made for Boys to use Jin Onuki's conventional sputtering method (Fig. 1(a)) as part of Boy's program (column 8, lines 54-69) for directing the operation of Boys' system by Boy's controller (57,58; Figure 1; column 8, lines 43-54).

Motivation for Boys to use Jin Onuki's conventional sputtering method (Fig. 1(a)) as part of Boys' program for directing the operation of Boys' system by Boys' controller is to deposit films for conventional "step coverage" and "electromigration resistance" as taught by Jin Onuki (abstract).

Even if we could agree with the Examiner that the proposed modification of Boys would be compatible with and a reasonable adjunct to the target wear compensating programmed control system of Boys, a significant difficulty we have with the Examiner's proposed modification is that the Examiner has not fairly established that Onuki teaches or suggests the desirability of providing a programmed control or set of computer readable memory instructions corresponding to those claimed at here.

In this regard, the Examiner refers to Figure 1a and the abstract of Onuki for teaching or suggesting such a programmed memory or controller for a plasma deposition apparatus. However, like Appellants, our review of Onuki, including the referred to sections thereof, does not reveal the teaching referred to by the Examiner. Rather, Onuki discloses deep followed by shallow bias sputtering as part of a so-called two step bias sputtering has certain advantages over conventional d.c and d.c. bias

sputtering (Abstract). Figure 1a of Onuki depicts a graph showing sputtering power and bias voltage waves for conventional DC sputtering and conventional DC bias sputtering. However, that drawing figure does not disclose or suggest alternating those conventional sputtering methods in forming coating layers on a substrate, as the Examiner alleges. Rather, Figure 1(a) of Onuki is more reasonably interpreted together with Figure 1(b) and the accompanying text of Onuki as disclosing either one-step switching or two-step switching bias sputtering, with no sputtering power supplied during bias, as alternatives to either of the conventional sputtering methods illustrated in Figure 1a. Thus, even if Onuki would be combinable with and suggest alternative instructions for use with the programmed memory for the controllers of Boys, those alternative instructions would not appear to result in a memory or controller combined with a set of plasma generation system control instructions as claimed at here.

On this record, we reverse the Examiner's obviousness rejection over Boys and Onuki.

Rejection of Claims 25-30 and 33-35

Dependent claims 25-30 and 33-35 are separately rejected over Boys taken with Onuki, as applied against claims 17-19, 31, and 32, further in view of Li. However, the Examiner has not explained how Li would make up for the deficiency in the rejection of independent claims 17 and 32 over Boys and Onuki, as discussed above. It follows that we shall also reverse this rejection.

Rejection of Claims 23, 24, and 36

Independent claim 23 is drawn to an integrated circuit including: (1) a plurality of active devices formed in a semiconductor substrate, (2) at least

one metal layer formed above the substrate, and (3) at least one insulating layer formed between the substrate and metal layer. The insulating layer includes a plurality of patterned holes filled with electrically conductive material to connect, selectively, the metal layer with substrate portions. The insulating layer includes first and second silicon oxide layers, each deposited via high-density chemical vapor deposition with the first layer deposited for mechanical stress reduction of the second layer.

The Examiner rejects claims 23, 24, and 36 as obvious, within the meaning of 35 U.S.C. § 103(a), over Onuki in view of Matsura. The Examiner maintains that Onuki discloses an integrated circuit substantially corresponding to the limitations of claim 23 but for the claimed insulating layer (Answer 13-14). The Examiner acknowledges that Onuki does not disclose an insulating layer including “a first silicon oxide layer and a second silicon oxide layer, said first and second silicon oxide layers deposited using a high-density plasma chemical vapor deposition process, said first silicon oxide layer deposited for the reduction of mechanical stress in said second silicon oxide layer” (Answer 13-14).² However, the Examiner maintains that “[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to perform film depositions by sputtering cycles of conventional sputtering (Fig. 1(a)) as taught by Onuki thereby depositing plural silicon oxide layers” (Answer 14).

² The Examiner does not maintain that the thermally grown insulation film of Onuki represents two layers of silicon oxide, as here claimed. Nor does the Examiner attempt to explain how Matsura, by itself, may or may not teach or suggest an integrated circuit as claimed without the Examiner’s proposed modification.

Appellants maintain that Onuki is directed to forming sputtered aluminum and aluminum alloy films whereas Matsura relates to deposition of silicon oxide films. Appellants assert that there is no suggestion in the applied references to apply the aluminum/aluminum alloy sputtering deposition technique of Onuki in forming a silicon oxide film as proposed by the Examiner in the stated rejection.

We agree with Appellants. Onuki is directed to forming interconnections for LSIs³ via a sputtering technique. Onuki does not address the applicability of their conductive metal interconnect forming technique to the formation of an insulating layer. On this record, the Examiner has not presented a persuasive rationale for the proposed combination of Onuki and Matsura as expressed in the Answer. In this regard, the Examiner's positioning of alleged teachings from Onuki concerned with interconnect formation in the same sentence with teachings from Matsura dealing with forming silicon oxide layers is not persuasive, of itself, to establish a motivation or suggestion for using the sputtering technique of Onuki in forming insulating layers, as asserted by the Examiner (Answer 16). Consequently, on this record, we reverse the Examiner's obviousness rejection of claims 23, 24, and 36 over the proposed combination of Onuki in view of Matsura.

³ LSIs, as used in Onuki, seems to be reasonably taken by the Examiner as referring to large-scale integration integrated circuits; that is, integrated circuits including a plurality of devices as required by rejected independent claim 23.

CONCLUSION

The Examiner's decision to reject claim 16 under 35 U.S.C. § 102 as being anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over Onuki; to reject claim 20 under 35 U.S.C. § 103(a) as being unpatentable over Li in view of Onuki; and to reject claims 21 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Li in view of Onuki and Boys is affirmed. The Examiner's decision to reject claims 17-19, 31, and 32 under 35 U.S.C. § 103(a) as being unpatentable over Boys in view of Onuki; and to reject claims 23, 24, and 36 under 35 U.S.C. § 103(a) as being unpatentable over Onuki in view of Matsura; and to reject claims 25-30, 33, 34, and 35 under 35 U.S.C. § 103(a) as being unpatentable over Boys and Onuki in view of Li is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2006).

AFFIRMED-IN-PART

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